What is Claimed is:

1. A nonvolatile ferroelectric memory device comprising:

a plurality of cell array blocks including a plurality of sub memory cell array blocks comprising a plurality of main bitlines and sub-bitlines connected to a plurality of memory cells;

a plurality of drivers for selecting the plurality of memory cells , respectively; and

a plurality of decoders connected to the cell array blocks, respectively, for applying decoding signals to the plurality of drivers,

wherein the decoder comprises a first sub-decoder for generating the decoding signal applied to the driver and a second sub-decoder for generating a signal selecting the driver.

2. The device according to claim 1, further comprising a current regulator which sets a potential of the main bitline as a voltage of the data by a voltage of data in the sub-bitline.

3. The device according to claim 2, wherein the current regulator comprises a transistor having a control terminal connected to the sub-bitline, a terminal connected to the main bitline and another terminal connected to a ground voltage.

4. The device according to claim 1, further comprising a pull-up means to pull up the sub-bitline as a boosting voltage.

5. The device according to claim 4, wherein the pull-up means comprises a transistor having a control terminal to receive a pull-up control signal, a terminal to receive pull-up signal and another terminal connected to the sub-bitline.

6. The device according to claim 5, wherein the pull-up signal transits to a boosting voltage in a predetermined time after the pull-up control signal transits to a boosting voltage.

7. The device according to claim 1, further comprising a switch means to interconnect the sub-bitline and the main bitline in restore and write operations.

8. The device according to claim 7, wherein the switch means is controlled by a control signal enabled to a boosting voltage in restore and write operation.

9. The device according to claim 1, further comprising a plurality of load controllers for controlling the main bitline to have a predetermined load value.

10. The device according to claim 1, wherein the driver is formed in a region where buses of output signals from the first sub-decoder and that of output signals from the second sub-decoder cross.

11. The device according to claim 10, wherein each driver comprises:

a first switch means for selectively transmitting a signal outputted from the first sub-decoder to a driving line in response to an output signal from the second sub-decoder; and

a second switch means for pulling down a driving line in response to another output signal from the second sub-

decoder.

12. The device according to claim 11, wherein each driver further comprises a third switch device for selectively transmitting the signal outputted from the second sub-decoder into a control terminal of the first switch means in response to a gate control signal.

13. The device according to claim 12, wherein the gate control signal includes a short pulse having a boosting voltage level.

14. The device according to one of claims 12 and 13, wherein the first sub-decoder further comprises a means for generating the gate control signal.

15. The device according to one of claims 12 and 13, wherein the second sub-decoder further comprises a means for generating the gate control signal.

16. The device according to claim 10, wherein the driver has a hierarchical signal line structure.

17. The device according to claim 16, wherein the

driver includes at lease one intermediate connecting layer for transmitting a signal outputted from the second sub-decoder.

18. The device according to claim 1, wherein the first sub-decoder includes a level shifter.

19. A nonvolatile ferroelectirc memory device comprising:

a plurality of unit memory blocks including one or more cell array blocks configured to include a plurality of sub-memory cell array blocks comprising a plurality of main bitlines and sub-bitlines connected to a plurality of memory cells, and the plurality of unit memory blocks including a sense amplifier array blocks including a plurality of sense amplifiers;

a plurality of drivers for selecting the memory cell of each cell array block; and

a plurality of decoders connected to each unit memory block and for applying decoding signals to the plurality of drivers,

wherein decoder comprises a first sub-decoder for generating the decoding signals applied to the driver, and a second sub-decoder for generating a signal for selecting

the driver;

wherein the plurality of unit memory blocks shares the second sub-decoder.

20. The device according to claim 19, wherein one or more of the cell array blocks share one sense amplifier array block.

21. A nonvolatile ferroelectric memory device comprising:

a plurality of cell array blocks including a plurality of sub-memory cell array blocks comprising a plurality of main bitlines and sub-bitlines connected to a plurality of memory cells;

a control circuit block including an address control circuit for controlling a store operation and a read operation,

wherein the address control circuit includes:

an address buffer for buffering an address pad signal inputted through an address pad in response to a clock enable signal;

an address latch for latching an output signal from the address buffer in response to an operation control signal; and

an address transition detector for detecting a transition point of an output signal from the address latch in response to the clock enable signal.

22. The device according to claim 21, wherein the address buffer includes:

a logic means for logically combining the address pad signal and the clock enable signal; and

a buffering means for buffering an output signal from the logic means.

23. The device according to claim 22, wherein the address buffer further comprises an ESD circuit connected to an input terminal to receive the address pad signal.

24. The device according to claim 21, wherein the address latch comprises:

a first transmitter for selectively transmitting an output signal from the address buffer in response to the operation control signal;

a latch means for latching an output signal selectively transmitted from the first transmitter; and

a second transmitter for selectively transmitting an output signal from the latch means into an input terminal

of the latch means in response to the operation control signal.

25. The device according to claim 24, wherein the address transition detector includes:

a delay means for delaying an signal outputted from the address latch for a predetermined time;

a logic means for logically combining an signal outputted from the address latch and an signal outputted from the delay means in response to the clock enable signal; and

a driver for outputting an address transition detecting signal configured to detect a transition point of an signal outputted from the address latch in response to an signal outputted from the logic means.

26. The device according to claim 25, wherein the driver includes a pull-down means for pulling down an address transition detecting signal in response to an signal outputted from the logic means.